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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,191	07/15/2003	Andrew S. Hildebrant	10030559-1	8661

7590 03/17/2006

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EXAMINER	
LE, DIEU MINH T	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 03/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,191	HILDEBRANT, ANDREW S.	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is response to the communication filed on 06/14/05 in application 10/624,470.

2. Claims 1-22 are presented for examination.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajsuman et al. (U.S. Patent 6,651,204 hereafter referred to as Rajsuman) in view of Nelson et al. (U.S. Patent 6,073,264 hereafter referred to as Nelson).

As per claim 1:

Rajsuman explicitly teaches the invention. Rajsuman teaches:

- A method for testing a device-under-test (DUT) [abstract, fig. 1-5, col. 1, lines 5-12 comprising the steps of:
- first plurality of data unit corresponding to a first plurality of DUT pins and second plurality of data unit corresponding to a second plurality of DUT pins [fig. 1-5, col. 3, line 30 through col. 4, line 20];
- separating the first plurality of data units from the second plurality of data units, wherein the first plurality of data units are communicated to the first plurality of DUT pins and the second plurality of data units are communicated to the second plurality of DUT pins [fig. 1-5, col. 3, line 30 through col. 4, line 56].

Rajsuman does not explicitly teach:
- examining a test data file that includes test data configured to enable testing the DUT.

However, Rajsuman does disclose capability of:

- A modular architecture for testing devices including memory and logic devices [abstract, fig. 1, col. 1, lines 6-12] comprising capabilities of:

- ***a testbench software tool used for producing test data including address data, write data, control data, timing data, etc…to supporting the device-under-test (DUT)*** [col.5, lines 24-30].

In addition, Nelson does explicitly disclose:

- A method and apparatus for debug ***the device-under-test (DUT)*** [abstract, fig. 1, col. 1, lines 33-45] comprising:

- ***designing, creating, and processing test data file comprising test data configuration, debugging connectivity, instrument setup, etc…*** [col. 6, lines 58 through col. 7, lines 28].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made first, to realize that the Rajsuman's ***a testbench software tool used for producing test data including address data, write data, control data, timing data, etc…to supporting the device-under-test*** capability does perform such Applicant's examining a test data file that includes test data configured to enable testing

the DUT limitation. This is because Rajsuman clearly applied these test data processes for testing configuration, simulation, evaluation DUT pins correspondences (i.e., examining) or connections in determining whether the system testing functioned properly; second, by applying the capabilities of ***designing, creating, and processing test data file comprising test data configuration, debugging connectivity, instrument setup, etc…*** as taught by Nelson in conjunction with the modular architecture for testing devices including memory and logic devices as taught by Rajsuman, the computer processing system, more specifically a testing ***device-under-test (DUT)*** can enhance its testing operation performance, more specifically to ensuring the error thoroughly detected and corrected via DUT testing including examining a test data file process.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to improve the computer testing system operation availability and network/system performance therein with a mechanism to enhance the data connectivity, data debugging, data displaying, data reliability, and data throughput which eventually will increase its performance, such as data throughput between internal and external devices.

As per claim 2:

Rajsuman explicitly teach the invention. Rajsuman teaches:

- the first plurality of data units have at least one different property than the second plurality of data units [fig. 1-5, col. 7, line 55 through col. 8, line 21].

As per claim 3:

Rajsuman explicitly teach the invention. Rajsuman teaches:

- the at least one different property includes timing complexity.

[fig. 1-5, col. 7, line 55 through col. 8, line 21 and col. 9, lines 21-25].

As per claims 4-5:

Rajsuman explicitly teach the invention. Rajsuman teaches:

- the at least one different property includes vector data volume.

[fig. 1-5, col. 7, line 55 through col. 8, line 21];

- the at least one different property includes repetitive data patterns (i.e., ***algorithmic patterns in a cycle based format***).

[fig. 1-5, col. 7, line 55 through col. 8, line 21 and col. 8, lines 48-60].

In addition, Nelson does explicitly disclose:

- A method and apparatus for debug ***the device-under-test (DUT)*** [abstract, fig. 1, col. 1, lines 33-45] comprising

- ***designing, creating, and processing test data file comprising test data configuration, debugging connectivity, instrument setup, etc…*** [col. 6, lines 58 through col. 7, lines 28].

- a debug test vector used for DUT testing [col. 1, lines 5-6];

- timing testing control capability in supporting the DUT testing [col. 4, lines 19-24];

- test data file format functionality in supporting the DUT testing [col. 6, lines 22-31].

As per claim 6:

Rajsuman further teaches:

- pin-unit groups assigning, testing, and configuring [fig. 1-5, col. 7, lines 56 through col. 8, lines 4].

Rajsuman does not explicitly teach:

- the first plurality of DUT pins are scan-pins and second plurality of DUT pins are non-scan pins.

However, Rajsuman does disclose capability of:

- A modular architecture for testing devices including memory and logic devices [abstract, fig. 1, col. 1, lines 6-12] comprising capabilities of:

- ***a testbench software tool used for producing test data including address data, write data, control data, timing data, etc…to supporting the device-under-test (DUT)*** [col.5, lines 24-30].

In addition, Nelson does explicitly disclose:

- A method and apparatus for debug ***the device-under-test (DUT)*** [abstract, fig. 1, col. 1, lines 33-45] comprising

- designing, creating, and processing test data file comprising test data configuration, debugging connectivity, instrument setup, etc… [col. 6, lines 58 through col. 7, lines 28].

- ***DUT scan output device capability in supporting the device-under-test (DUT)*** [col. 6, lines 17-20 and col. 7, lines 20-27].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to apply the capability ***DUT scan output device capability in***

supporting the device-under-test (DUT) as taught by Nelson in conjunction with the modular architecture for testing devices including memory and logic devices as taught by Rajsuman, the computer processing system, more specifically a testing ***device-under-test (DUT)*** can enhance its testing operation performance, more specifically to ensuring the error thoroughly detected and corrected via DUT testing including examining a test data file process.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to improve the computer testing system operation availability and network/system performance therein with a mechanism to enhance the data connectivity, data debugging, data displaying, data reliability, and data throughput .

As per claim 7:

Rajsuman explicitly teach the invention. Rajsuman teaches:

- formatting the first plurality of data units independently from the second plurality of data units [fig. 1-5, col. 8, lines 5-15].

As per claim 8:

Rajsuman explicitly teach the invention. Rajsuman teaches:

- the test data file is one of a STIL (standard test interface language) file and a WGL (waveform generation language) file [fig. 3, col. 6, lines 25-35];

As per claim 9:

Rajsuman explicitly teach the invention. Rajsuman teaches:

- at least one processor operating in a first timing domain enables the first plurality of data units to be provided to the first plurality of DUT pins, and at least one processor operating in a second timing domain enables second plurality of data units to be provided to the second plurality of DUT pins, wherein the second timing domain is different from the first timing domain [fig. 4, col. 6, lines 37-65; col. 7, line 55 through col. 8, line 21; col. 9, lines 20-25; and col. 10, lines 40-41].

In addition, Nelson does explicitly disclose:

- A method and apparatus for debug ***the device-under-test (DUT)*** [abstract, fig. 1, col. 1, lines 33-45] comprising

- ***designing, creating, and processing test data file comprising test data configuration, debugging connectivity, instrument setup, etc...*** [col. 6, lines 58 through col. 7, lines 28].

- a debug test vector used for DUT testing [col. 1, lines 5-6];

- timing testing control capability in supporting the DUT testing [col. 4, lines 19-24];

- test data file format functionality in supporting the DUT testing [col. 6, lines 22-31].

As per claims 10-15:

These claims are the same as per claims 1-9. The only minor different is that claim 10 introduces a capability of ***storing*** information identifying first plurality of DUT pins in ***memory***. However, Rajsuman explicitly teaches ***a memory for storing and testing the device-under-test (DUT) including timing*** [abstract, col. 2, lines 28-32; col. 8, lines 43-47; and col. 10, lines 40-41]; Therefore, these claims are also rejected under the same rationale applied against claims 1-9.

As per claims 16-18:

These claims are the same as per claims 1-9. The only minor different is that claim 10 introduces a ***memory*** capability for ***storing*** test data file. However, Rajsuman explicitly teaches ***a memory for storing and testing the device-under-test (DUT) including timing*** [abstract, col. 2, lines 28-32; col. 8, lines

43-47; and col. 10, lines 40-41]; Therefore, these claims are also rejected under the same rationale applied against claims 1-9.

As per claims 19-21:

Due to the similarity of claims 19-21 to claims 16-18 except for a system for testing a device-under-test (DUT) comprising a memory operative to store a test data file, a processor programmed to identifying the first plurality of DUT pins, etc… instead of a method for testing a device-under-test (DUT) comprising a memory operative to store a test data file, a processor programmed to identifying the first plurality of DUT pins, etc…; therefore, these claims are also rejected under the same rationale applied against claims 16-18. **In addition, all of the limitations have been noted in the rejection as per claims 16-18.**

As per claim 22:

Due to the similarity of claim 22 to claim 16 except for a system for testing a device-under-test (DUT) comprising a **means** operative to store a test data file, a **means** programmed to identifying the first plurality of DUT pins, etc… instead of a method for testing a device-under-test (DUT) comprising a memory

operative to store a test data file, a processor programmed to identifying the first plurality of DUT pins, etc…; therefore, this claim is also rejected under the same rationale applied against claim 16. **In addition, all of the limitations have been noted in the rejection as per claim 16.**

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. A shortened statutory period for response to this action is set to expired THREE (3) months, ZERO days from the date of this letter. Failure to respond within the period for response will cause the application to be abandoned. 35 U.S.C. 133.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (571) 272-3660. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be

reached on (571)272-3644. The Tech Center 2100 phone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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PRIMARY EXAMINER
ART UNIT 2114

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